REMARKS

Applicants respectfully request reconsideration and allowance of the subject application.

Claims 1-23 were originally submitted

Claims 9, 14, and 21 were previously amended.

Claims 24 and 25 were previously added.

No claims are canceled.

Claims 4, 15, and 17 are currently amended.

Claims 1-25 remain in this application.

35 U.S.C. §102

Claims 1, 14, 24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,085,333 to DeKoning et al (DeKoning). Reconsideration is requested.

DeKoning teaches a RAID storage subsystem 100, having redundant disk array controllers (RDAC) 118.1 and 118.2. One RDAC acts as primary controller and the other RDAC acts as a redundant controller. Each RDAC 118.1 and 118.2 is connected to a disk array 108 via bus (or busses) 150 and to host computer 120 via a separate bus 154. (DeKoning, col. 5 lines 14-23)

RDAC 118.1 includes a main CPU 112.1, a flash memory 114.3 and a program memory 114.1 for storing program instructions and variables for the operation of a CPU 112.1, a local memory 116.1 (i.e., cache memory) for storing data and control information related to the data stored in disk array 108, and a RAID Parity Assist (RPA) 113.1 memory. RDAC 118.1 also includes a co-processor 115.1 for controlling transfer of data to and from disk drives 110. Co-

processor 115.1 is an inter-controller communication chip (ICON) application specific integrated circuit (ASIC) that provides communication and coordination for the transfer of data between the native controller's (i.e., RDAC 118.1) RPA memory 113.1 to the spare controller's (i.e., RDAC 118.2) RPA memory 113.2 without assistance of the CPU 112.1. In this case, the ICON ASIC (i.e., co-processor 115.1) executes application specific code which includes a set of address ranges to perform data transfers. CPU 112.1, flash memory 114.4, program memory 114.1, cache memory 116.1, and co-processor 115.1 are connected via memory bus 152.1 to enable CPU 112.1 to store and retrieve information in the memory devices 116.1, 114.1. (DeKoning col. 5 line 56 to col. 6 line 9).

RDAC 118.2 is identical to RDAC 118.1. RDAC 118.2 includes a CPU 112.2, a flash memory 114.4, a program memory 114.2, a cache memory 116.2, RPA memory 113.2, and a co-processor 115.2, all interconnected via memory bus 152.2. To permit each RDAC to communicate with the other, the RDACs 118.1 and 118.2 are interconnected via a shared bus 156. (DeKoning col. 6 lines 54-59).

Independent claim 1, for example, recites "[a] data array system for providing a host computer device having a host bus redundant access to a data storage device, comprising:

> an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and
>
> a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link.

The Action looks to DeKoning and argues that either RDAC 118.1 or 118.2 as an active controller that is linked to the host bus 154 and disk array 108. The Action also argues that either RDAC 118.1 or 118.2, as an active controller, and specifically CPU 112 and associated circuitry includes a messaging system for transmitting the messages and data over the host bus 154 and a standby controller, either RDAC 118.1 or 118.2, linked to the host bus 154 and the data array 108 (data storage device). The Action further argues that the standby controller includes message and data buffers (respective memory 114 or 116) for storing the messages and data, whereby the host bus functions as functions as an inter-controller link (the Action citing Figs. 1, 3, and col. 6 lines 9-67 of Dekoning).

The Action further presents that the CPU and co-processor of RDAC 118.1 or 118.2 as a messaging mechanism. The Applicant argued in a previous response, that the CPUs taught in DeKoning communicate to their respective co-processors via a memory bus (e.g., bus 152.1 and 152.2). The co-processors are used to communicate transfer of data between one another's RPA memories. The co-processors are interconnected via a shared bus 156. The messaging is not over the host bus 154, but through the separate and distinct shared bus 156. Therefore, DeKoning fails to teach the element "a messaging mechanism for transmitting the messages over the host bus".

Claim 1 particularly recites "a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link".

As discussed above and argued in a previous response, the RDACs 118.1 and 118.2 communicate with one another over the separate and distinct shared bus

156, not over bus 154. Therefore, DeKoning fails to teach the element "the host bus functions as an inter-controller-link". The Action indicates that the "Applicant's arguments regarding the host bus functions as an inter controller link between controllers have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new ground(s) of rejection (for claims 1-3, 14, 20, 24, and 25) is made in view of another embodiment taught by DeKoning". The Action cites Figs. 1, 3, and col. 6 lines 9-67 of DeKoning as teaching this element; however, this particular section (another embodiment taught by DeKoning) does not disclose that the host bus 154 allows the RDACs 118.1 and 118.2 to communicate with one another. What is disclosed in the cited section is that in order "[t]o permit each RDAC to communicate with the other, the RDACs 118.1 and 118.2 are interconnected via shared bus 156". (DeKoning, col. 6 lines 57-59).

Accordingly, DeKoning does not show every element of claim 1, and the rejection of claim 1 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 1 be withdrawn.

Independent claim 14 recites in part "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus".

As discussed above, RDACs 118.1 and 118.2 are linked with one another communicate with one another over the separate and distinct shared bus 156, not bus 154. Therefore, DeKoning does not disclose inter-controller communications over the host bus (i.e., bus 154) as recited in claim 14.

Accordingly, DeKoning does not show every element of claim 14, and the rejection of claim 14 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 14 be withdrawn.

Independent claim 24 recites in part "an active controller linked to the host bus and the at least one data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and, a standby controller linked to the host bus and the at least one data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link configured to transfer data and message information between the active and standby controllers and wherein upon a failure of the active controller the inter-controller-link provides both data and message transfer within the computing device such that the host CPU can cause the standby controller to access data from the at least one data storage device".

The Action presents that the CPU and/or co-processor of RDACs 118.1 or 118.2 as a messaging mechanism that transmits over a host bus or bus 154; however, as discussed above the CPU and/or co-processor do not transmit over bus 154. Therefore, DeKoning does not teach the element "a messaging mechanism for transmitting the messages and data over the host bus" as recited by claim 24.

As discussed above, RDACs 118.1 and 118.2 are linked with one another communicate with one another over the separate and distinct shared bus 156, not bus 154. Therefore, DeKoning does not disclose "the host bus functions as an inter-controller-link configured to transfer data and message information between the active and standby controllers" as recited in claim 24.

Accordingly, DeKoning does not show every element of claim 24, and the rejection of claim 24 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 24 be withdrawn.

Independent claim 25 recites in part "an active controller sub-system linked directly to the host bus and the data storage device, the active controller sub-system including a messaging mechanism for transmitting messages and data over the host bus; and, a standby controller sub-system linked directly to the host bus and the data storage device, the standby controller sub-system including message and data buffers for storing the messages and data, whereby the host bus functions as a redundant inter-controller-link such that upon failure of either of the active controller subsystem and the standby controller sub-system the host computing device maintains access to the data storage device".

Similar arguments are presented by the Action in rejecting claim 25 as to rejecting claim 24. Applicants present arguments in support of claim 25 used in support of claim 24. In particular, Applicants present that DeKoning does not teach "a messaging mechanism for transmitting messages and data over the host bus" and "the host bus functions as a redundant inter-controller-link such that upon failure of either of the active controller subsystem and the standby controller sub-system the host computing device maintains access to the data storage device" as recited in claim 25.

Accordingly, DeKoning does not show every element of claim 25, and the rejection of claim 25 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 25 be withdrawn.

35 U.S.C. §103

Claims 2-3 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of U.S. Patent No. 6,094,699 to Surugucchi et al. (Surugucchi). Reconsideration is requested.

Claims 2-3 depend from claim 1, and therefore include the elements of "an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus" and "a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link".

The Action relies on the arguments as to claim 1, relying on DeKoning. However, as discussed above in support of claim 1, DeKoning fails to teach the elements of claim 1.

Surugucchi is cited for teaching "PCI bus connecting PCI-compliant RAID controllers (col. 1 lines 19-27)"; however, Surugucchi provides no assistance in light of DeKoning as to the recited methodology of claim 1. Accordingly, DeKoning and Surugucchi individually or considered together fail to teach or suggest every element of claims 2-3, and the rejection of claims 2-3 is therefore improper. Applicants respectfully request that the §103 rejection of claims 2-3 be withdrawn.

Claim 20 depends on claim 14, and therefore includes the element "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy

messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus".

The Action relies on the arguments as to claim 1 (claim 14), relying on DeKoning. However, as discussed above in support of claim 14, DeKoning fails to teach the particular element of claim 14.

Surugucchi is cited for teaching "PCI bus connecting PCI-compliant RAID controllers (col. 1 lines 19-27)"; however, Surugucchi provides no assistance in light of DeKoning as to the recited system of claim 14. Accordingly, of DeKoning and Surugucchi considered individually or together fail to teach or suggest every element of claim 20, and the rejection of claim 20 is therefore improper. Applicants respectfully request that the §103 rejection of claim 20 be withdrawn.

Allowable Subject Matter

Claims 9-13 and 21-23 are allowed. Applicant appreciates the allowance of the claims.

Claims 4-8 and 15-19 are objected to as being depending upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Claims 4-8 and 15-19 have been amended where necessary to overcome the objection. Applicant appreciates the allowance of the claims.

CONCLUSION

All pending claims 1-25 are in condition for allowance. Applicants respectfully request reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Dated: 1/13/06 By: _____

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